THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte EITAN ROSEN and JACK DOWECK

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Appeal No. 1997-0556
Application No. 08/286,265

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ON BRIEF

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Before BARRETT, FLEMING, and DIXON, **Administrative Patent Judges**.

DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 19-30, which are all of the claims pending in this application.

We REVERSE.

BACKGROUND

The appellants' invention relates to a N-way set-associative cache memory which includes a store hit buffer for improved data access. The store hit buffer recognizes when the processor requests data stored in the buffer and substitutes the buffered data for data from the memory array. An understanding of the invention can be derived from a reading of exemplary claim 19, which is reproduced below.

19. An N-way, set associative cache memory comprising:

a memory array having N sets of data bit lines and N sets of associated address tag bit lines;

an addressing circuit which generates a tag compare address and a set address for a read operation, and write control signals for a write operation;

N amplifier circuits, each of which is coupled to corresponding sets of the data/address tag bit lines of the memory array, each of the N amplifier circuits having outputs which provide data and address tags sensed from the respective data/address tag bit lines of the memory array;

N read/write (R/W) circuits, each of which is correspondingly coupled to the outputs of the N amplifier circuits and also to the addressing circuit, each of the R/W circuits comprising:

a buffer circuit for buffering write data/address information preceding a write operation, the buffer circuit including a comparator which generates a set compare result when the set address matches the write address;

comparator means for comparing the address tags sensed by the N amplifier circuits with the tag compare address to produce a match signal; and

multiplexer means controlled by the set compare result and match signal for selecting as a cache output either a write data bit from the buffer circuit or a data bit sensed from the memory array.

The prior art references of record relied upon by the examiner[1] in rejecting the appealed claims are:

Rosich 5,224,214 Jun. 29, 1993

Patterson et al. (Patterson), "Computer Architecture: A Quantitative Approach", Chapter 8.3, pp 408-417, published by Morgan Kaufmann Publishers, Inc. (1990)

Claims 19-30 stand rejected under 35 U.S.C. § 103 as being unpatentable over Rosich in view of Patterson.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 12, mailed Aug. 7, 1996) for the examiner's reasoning in support of the rejections, and to the appellants' brief (Paper No. 11, filed May 13, 1996) for the appellants' arguments thereagainst.

[1] We note that the examiner lists Rosich '660 and Stamm '918 on page 4 of the answer as new prior art, but does not rely upon these references in the rejection or response to arguments. Similarly, these references form no part of our consideration.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by appellants and the examiner. As a consequence of our review, we make the determinations which follow.

Appellants argue that the two references are fundamentally different and incompatible. (See brief at page 9.) We agree with appellants to the extent that the Rosich reference emphasizes the teaching concerning the main memory read procedure and briefly addresses the updating of the cache memory while the other reference to Patterson is only concerned with teaching the narrow area concerning the cache operation. In our view, the examiner has not provided a motivation in the individual references, a statement of the general knowledge in the art or a convincing line of reasoning why one skilled artisan would have been motivated to combine the distinct teachings.

Appellants argue that the present invention solves a problem in the art con-cerning the merging of buffer data with cache array data for read operations without causing delays. Appellants' solution involves adding circuitry to the cache to substitute the buffer data for the cache array data if the data are located in the buffer. (See brief

at page 9.) We agree with appellants that the language of the independent claims 19, 24, and 29 expressly set forth limitations to the read/write buffer in the cache memory which solve this problem. The examiner repeatedly cites to the same portions of Rosich and maintains that skilled artisans would have been motivated to incorporate the read/write buffer for main memory read conflicts into the cache memory to address read conflicts therein. (See answer at pages 8-20.) We do not agree with the examiner. Appellants argue that Rosich was aware of cache memories since a cache memory is included in the system of Rosich, but the read/write buffer was not included into the cache memory. Therefore, if the inclusion of the read/write buffer and substitution were as apparent as the examiner implies, then Rosich would have similarly included such a feature in the cache memory. (See brief at pages 10 and 11.) On its face, we agree with the appellants' rationale rather than the examiner's unsupported conclusion, which in our view uses hindsight in an attempt to reconstruct the claimed invention. The examiner has not provided any cogent line of reasoning for skilled artisans to extend the teachings of Rosich with respect to main memory to another subsystem therein which does not teach or suggest a need for this additional savings with respect to a clock signal. Therefore, we cannot sustain the rejection of independent claims 19, 24, and 29 and their respective dependent claims.

CONCLUSION

To summarize, the decision of the examiner to reject claims 19-30 under 35 U.S.C. § 103 is reversed.

REVERSED

LEE E. BARRETT Administrative Patent Judge	)))))) BOARD OF PATENT
MICHAEL R. FLEMING Administrative Patent Judge	) APPEALS) AND) INTERFERENCES
JOSEPH L. DIXON Administrative Patent Judge	))))

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